Remarks

The non-final Office Action dated September 8, 2009 lists the following rejections: claims 1-3, 6-7, 10 and 12-17 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Suzuki (EP 1 046 983) in view of Faraboschi (U.S. Patent No. 5,930,508); and claims 8-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the '983 reference in view of the '508 reference as applied to claim 1, and further in view of Iwata (U.S. Pat No. 6,275,921) and Topham (U.S. Patent Pub. 2001/0047466). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant appreciates the Examiner's response to arguments, but notes that the Examiner's interpretation improperly truncates limitations thereby failing to consider the limitations as a whole and is insufficient to establish a *prima facie* case. In particular, the Examiner goes to great lengths to explain the asserted interpretation of limitations directed toward "indicating a sequential order." The interpretation, however, fails to consider the entirety of the claim limitations, which relate to the sequential order of "instructions at their respective functional units." The Examiner's interpretation is unrelated to an instruction order at the functional units as the delimiters and the Examiner's explanation simply separate two compacted instructions within memory. Thus, the Examiner's interpretation is improperly based upon the sequential status of boundaries within memory rather than an order of instructions at their respective functional units.

Moreover, the delimiters do not indicate an order. The Examiner's alleged sequential order relates to an order of instructions as stored in memory. Regardless of the existence of delimiters, this order exists and the delimiters do not provide an indication of this order. A careful review of the Faraboschi reference shows that no value of the delimiters affects or indicates what the sequential order is as it is always just the order of storage in memory. Thus, while the use of the delimiters relates, tangentially, to accessing the instructions from memory, the delimiters do not provide indications of an order as the order is defined by storage locations within the memory. Indeed, any order could exist and the delimiters would not change value and conversely the value of the

delimiters provides no data that indicates what the sequential order is or is not. Simply because instructions may or may not be accessible without the use of delimiters, the delimiters do not provide an indication of a sequential order that is defined entirely by the order of instructions within memory. Thus, the Examiner's basis for the interpretation is erroneous in that the delimiters are not "used to determine a sequential order," any more than power to the circuit is "used to determine a sequential order" (*e.g.*, you don't know where one instruction ends and where a next begins unless you have sufficient electrical power to access the memory circuit). Accordingly, the Examiner's interpretation is improper as the skilled artisan would readily understand that power to the circuit does not indicate a sequential order, and more importantly, that the identified delimiters do not indicate a sequential order.

Moreover, the Examiner's interpretation fails to show correspondence in other aspects. Claim limitations are directed toward indication of sequential order of specific instructions within a new single instruction. The delimiters are used to separate already compacted instructions and do not separate instructions within the same compacted instruction. As the claim limitations are directed toward a sequence of two instructions within a single instruction, the Examiner's interpretation is erroneous. That is to say that to the extent any two instructions are compacted into a single instruction, the delimiters do not indicate an order thereof. Instead, the delimiters are used to separate compacted instructions and therefore do not indicate sequential order of instructions contained within the compacted instructions. Accordingly, Applicant maintains that because the delimiter encoding bits merely indicate boundaries between compacted instructions, there is not a *prima facie* case of correspondence.

Applicant also submits that the Examiner's characterization that "Fabroschi provides clear motivation" is not supported by the record. The Examiner's allegedly "clear motivation" is to provide "more efficient compression," however the record does not show that Fabroschi provides more efficient compression when compared to the '983 reference. The Examiner's only identified modification to the '983 reference is to add control information to the already compressed instructions of the '983 reference. Since the addition of control information would result in increased data size, the Examiner's alleged motivation is expressly defeated by the proposed modification.

Moreover, the '983 reference uses a different scheme that does not require the use of the delimiters for the Fabroschi reference. Neither the Examiner nor the references teach or suggest that these different schemes would function together. Applicant respectfully submits that a proper obviousness rejection requires a "clearly articulated" explanation for the combination. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (U.S. 2007). As the '983 reference implements a first compression scheme and the Fabroschi reference implements a second compression scheme, the Examiner has incorrectly concluded, without sufficient articulated explanation thereof, that individual elements of one compression scheme have usefulness in the other. Applicant notes that the compression schemes rely upon different types of coding of the data and would not be a simple one-for-one replacement or integration of elements from one into the other. Accordingly, there is not a *prima facie* showing of obviousness due to the absence of any clearly articulated details regarding how the combination would function.

In this regard, Applicant also notes that the Examiner is relying extensively upon the compression technique of the '983 reference to show correspondence, thereby making it improper to replace this compression technique with that of another technique. That is to say, if the compression techniques of the '983 reference are no longer present, then those aspects relied upon are also absent.

The Examiner's attempt to dismiss evidence of non-obviousness in the form of teaching away and frustration of purpose is misguided. It is not proper to ignore such factors based upon novel theories and attempts to discount established precedent as unimportant. As correctly noted in *KSR*, it is nearly always possible to find every claim element, in some form or another. *KSR* at 419. Other guidelines recognize that an examiner is necessarily afforded with knowledge of the invention, opening the door for improper hindsight reconstruction. For these and other reasons, the case law clearly prohibits combinations that would so change the underlying reference that it would cease to operate according to the primary teachings. The case law also clearly establishes that teaching away is strong evidence of non-obviousness. As such, combinations that redesign the underlying teachings in a manner that undoes stated objectives thereof are *prima facie* invalid irrespective of whether or not they might or might not be possible.

In this particular instance, the Examiner alludes to an unidentified and hypothetical compression scheme based upon "compressed instructions that do not need to meet the same criteria that instructions in the system of Suzuki must meet in order to be compressed." Respectfully, neither the references nor the Examiner teach or suggest such a combination. Applicant submits that the mere addition of delimiter encoding bits into the system of the '983 reference would not provide the stated benefits and would frustrate the purpose of the '983 reference. For instance, the '983 reference has not been shown to suffer from problems related to storage of instruction words across address boundaries. Fig. 3 of the '983 reference shows that the system is designed so that the stored instructions 15 can be easily transferred to respective left and right containers 2,3. This is accomplished through a specific coding and compression scheme discussed in detail in the '983 reference. In contrast, the Fabroschi reference uses a very different scheme that is not designed in a manner consistent with the '983 reference's simple transfer to respective left and right containers. As such, the Fabroschi reference is subject to problems that do not exist in the context of the '983 reference. The combination is therefore improper because the skilled artisan would not seek to modify the '983 reference to fix problems that do not exist. Thus, the proposed modification serves no identifiable purpose and appears only to increase the size of the instruction in direct contradiction to a stated purpose of the '983 reference. Moreover, a hypothetical and significant redesign of the '983 reference would be *prima facie* invalid as the resulting system would cease to function consistent with the functionality taught by the '983 reference.

For the aforementioned reasons, the proposed modification is illogical and cannot be read on the claimed invention when viewed as a whole.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062 (or the undersigned).

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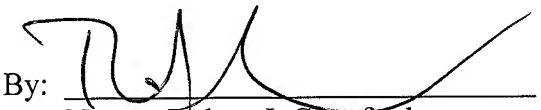
By: 

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